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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/697,364	10/26/2000	Sally S. Botala	BUR9-2000-0157-US1	3655

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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
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ESSEX JUNCTION, VT 05452

EXAMINER

TORRES, JOSEPH D

ART UNIT	PAPER NUMBER
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2133

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DATE MAILED: 10/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary

Application No.

09/697,364

Applicant(s)

BOTALA ET AL.

Examiner

Joseph D. Torres

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-27 is/are rejected.
- 7) ☒ Claim(s) 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 October 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to newly added claims 19-27 have been considered but are moot in view of the new ground(s) of rejection.

Note: Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Claim Objections

2. Claim 21 is objected to because of the following informalities: claim 21 depends from canceled claim 1. The Examiner assumes that the Applicant intended claim 21 to depend from claim 19. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 19-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Turnquist, James Alan (US 6557128 B1).

35 U.S.C. 102(e) rejection of claim 19.

Turnquist teaches a method of automatically generating a test environment for an ATE, designed to test a single integrated circuit (col. 1, lines 7-12 in Turnquist teach that the invention in Turnquist is directed to a single ATE system, which behaves as multiple logic testers), the method comprising the steps of: mapping the pins of the ATE to a plurality of integrated circuits to create pin data (Claim 2 of Turnquist teaches pin-units are assigned to test pins based on a group selection address; col. 5, lines 32-35 in Turnquist teach that the host control system 31 in Figure 3 controls the mapping assignment of pin units by creating and transmitting a group select address to the pin-unit write decoder 53 in Figure 4 contained in each pin-unit 35 in Figure 3; Note: group select addresses are pin data); automatically generating, with a test program generator, a test program (Step S13 in Figure 8 is a step for generating a test program, see col. 8, lines 5-15 in Turnquist for details; in col. 8, lines 1-4, Turnquist teaches that test programs for parallel testing are accomplished by the batch loaded handler of Figure 2B using the simple algorithm of Figure 8, hence the batch loaded handler of Figure 2B is a test program generator for automatically generating instantiations of test programs) and test pattern data for the integrated circuits (col. 3, lines 10-12 in Turnquist teach that each pin unit has a means for generating a test pattern) from pattern data (col. 5, lines 16-25 in Turnquist teach the test patterns are generated based on test data for cycle

based testing for which the tester in Turnquist is made for, hence test data is pattern data), generic test program rules (the Algorithm in Figure 8 in Turnquist is a group of generic test program rules used to generate instantiations of test programs), and the pin data (col. 5, lines 32-35 in Turnquist teach that the host control system 31 in Figure 3 controls the mapping assignment of pin units by creating and transmitting a group select address to the pin-unit write decoder 53 in Figure 4 contained in each pin-unit 35 in Figure 3; Note: group select addresses are pin data); and executing the test program to control the ATE (see Abstract in Turnquist; Note: Turnquist teaches that overall control of the test system is executed by a test program during testing).

35 U.S.C. 102(e) rejection of claim 20.

Turnquist teaches generating functional fail data for each of the integrated circuits (col. 5, lines 9-10 in Turnquist; Note: read pattern fail addresses is functional fail data).

35 U.S.C. 102(e) rejection of claim 21.

Turnquist teaches the test program includes test vectors and pin assignments for testing the integrated circuits in parallel (see Figure 12 and col. 4, lines 13-16 in Turnquist, Note: Figure 12 is an algorithm for assigning a group of virtual logic testers prior to the parallel testing).

35 U.S.C. 102(e) rejection of claim 22.

Turnquist teaches automated test system comprising: an integrated circuit tester designed to test a single integrated circuit (col. 1, lines 7-12 in Turnquist teach that the invention in Turnquist is directed to a single ATE system, which behaves as multiple logic testers); a pin data storage area capable of containing pin data for mapping a plurality of integrated circuits to the pins of the integrated circuit tester (Group Selection Address Register 41 in Figure 4 of Turnquist is a pin data storage area capable of containing pin data for mapping a plurality of integrated circuits to the pins of the integrated circuit tester; Note: Claim 2 of Turnquist teaches pin-units are assigned to test pins based on a group selection address; col. 5, lines 32-35 in Turnquist teach that the host control system 31 in Figure 3 controls the mapping assignment of pin units by creating and transmitting a group select address to the pin-unit write decoder 53 in Figure 4 contained in each pin-unit 35 in Figure 3; Note: group select addresses are pin data); a generic program rules storage area (col. 5, lines 45-48 in Turnquist teach that instructions, i.e., generic program rules, are allowed to reach inner registers; Note: registers are storage units); and a test program generator capable of generating a test program (Step S13 in Figure 8 is a step for generating a test program, see col. 8, lines 5-15 in Turnquist for details; in col. 8, lines 1-4, Turnquist teaches that test programs for parallel testing are accomplished by the batch loaded handler of Figure 2B using the simple algorithm of Figure 8, hence the batch loaded handler of Figure 2B is a test program generator for automatically generating instantiations of test programs) from the pin data (col. 5, lines 32-35 in Turnquist teach that the host control system 31 in Figure 3 controls the mapping assignment of pin units by creating and transmitting a

group select address to the pin-unit write decoder 53 in Figure 4 contained in each pin-unit 35 in Figure 3; Note: group select addresses are pin data), test pattern data (col. 5, lines 16-25 in Turnquist teach the test patterns are generated based on test data for cycle based testing for which the tester in Turnquist is made for, hence test data is test pattern data) and generic program rules (the Algorithm in Figure 8 in Turnquist is a group of generic test program rule used to generate instantiations of test programs), the test program capable of controlling the integrated circuit tester for testing the integrated circuits in parallel (see Abstract in Turnquist; Note: Turnquist teaches that overall control of the test system is executed by a test program during testing; see Figure 12 and col. 4, lines 13-16 in Turnquist, Note: Figure 12 is an algorithm for assigning a group of virtual logic testers prior to the parallel testing).

35 U.S.C. 102(e) rejection of claim 23.

Turnquist teaches a storage area capable of storing fail data generated during testing for each one of the integrated circuits (Fail Memory 18 in Figure 1 of Turnquist is a storage area capable of storing fail data generated during testing; Note: the Turnquist invention only alters the delivery system to allow a conventional ATE to test multiple ICs in parallel, hence the ATE in Turnquist must inherently have Fail Memory since fail memory is a part of the conventional ATE as taught in Turnquist).

35 U.S.C. 102(e) rejection of claim 24.

Turnquist teaches the test program includes test vectors and pin assignments for testing the integrated circuits in parallel (see Figure 12 and col. 4, lines 13-16 in Turnquist, Note: Figure 12 is an algorithm for assigning a group of virtual logic testers prior to the parallel testing).

35 U.S.C. 102(e) rejection of claim 25.

Turnquist teaches a computer program product (see Abstract in Turnquist: Note: Turnquist teaches a host computer for executing a test program) comprising: a computer usable medium having computer readable program code embodied in the medium for automatically generating a test environment for an integrated circuit tester when executed, the computer readable program code including (col. 5, lines 7-10 of Turnquist teach that the host computer controls the overall operation of the test system): computer readable program code that is capable of mapping the pins of the integrated circuit tester to a plurality of integrated circuits to create pin data (Claim 2 of Turnquist teaches pin-units are assigned to test pins based on a group selection address; col. 5, lines 32-35 in Turnquist teach that the host control system 31 in Figure 3 controls the mapping assignment of pin units by creating and transmitting a group select address to the pin-unit write decoder 53 in Figure 4 contained in each pin-unit 35 in Figure 3; Note: group select addresses are pin data); and computer readable program code that is capable of automatically generating, with a test program generator, a test program (Step S13 in Figure 8 is a step for generating a test program, see col. 8, lines 5-15 in Turnquist for details; in col. 8, lines 1-4, Turnquist teaches that test programs for parallel

testing are accomplished by the batch loaded handler of Figure 2B using the simple algorithm of Figure 8, hence the batch loaded handler of Figure 2B is a test program generator for automatically generating instantiations of test programs) and test pattern data for the integrated circuits (col. 3, lines 10-12 in Turnquist teach that each pin unit has a means for generating a test pattern) pattern data (col. 5, lines 16-25 in Turnquist teach the test patterns are generated based on test data for cycle based testing for which the tester in Turnquist is made for, hence test data is pattern data), generic test program rules (the Algorithm in Figure 8 in Turnquist is a group of generic test program rule used to generate instantiations of test programs), and the pin data (col. 5, lines 32-35 in Turnquist teach that the host control system 31 in Figure 3 controls the mapping assignment of pin units by creating and transmitting a group select address to the pin-unit write decoder 53 in Figure 4 contained in each pin-unit 35 in Figure 3; Note: group select addresses are pin data); and executing the test program to control the ATE (see Abstract in Turnquist; Note: Turnquist teaches that overall control of the test system is executed by a test program during testing).

35 U.S.C. 102(e) rejection of claim 26.

Turnquist teaches generating functional fail data for each of the integrated circuits (col. 5, lines 9-10 in Turnquist; Note: read pattern fail addresses is functional fail data).

35 U.S.C. 102(e) rejection of claim 27.

Turnquist teaches the test program includes test vectors and pin assignments for testing the integrated circuits in parallel (see Figure 12 and col. 4, lines 13-16 in Turnquist, Note: Figure 12 is an algorithm for assigning a group of virtual logic testers prior to the parallel testing).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sugamori, Shigeru (US 6536006 B1) teaches a test system formed by freely combining a plurality of tester modules having identical or different capabilities where each of the tester module operates independently from one another thereby being able to test an analog signal block and a digital signal block of the device under test at the same time.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

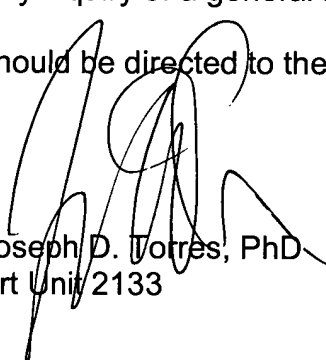
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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

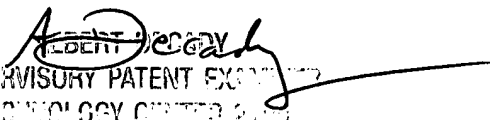
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



Joseph D. Torres, PhD
Art Unit 2133



ALBERT DECADY
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